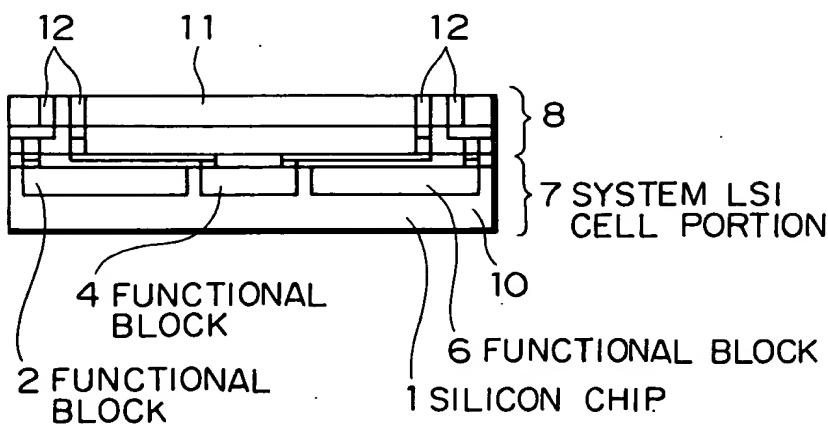
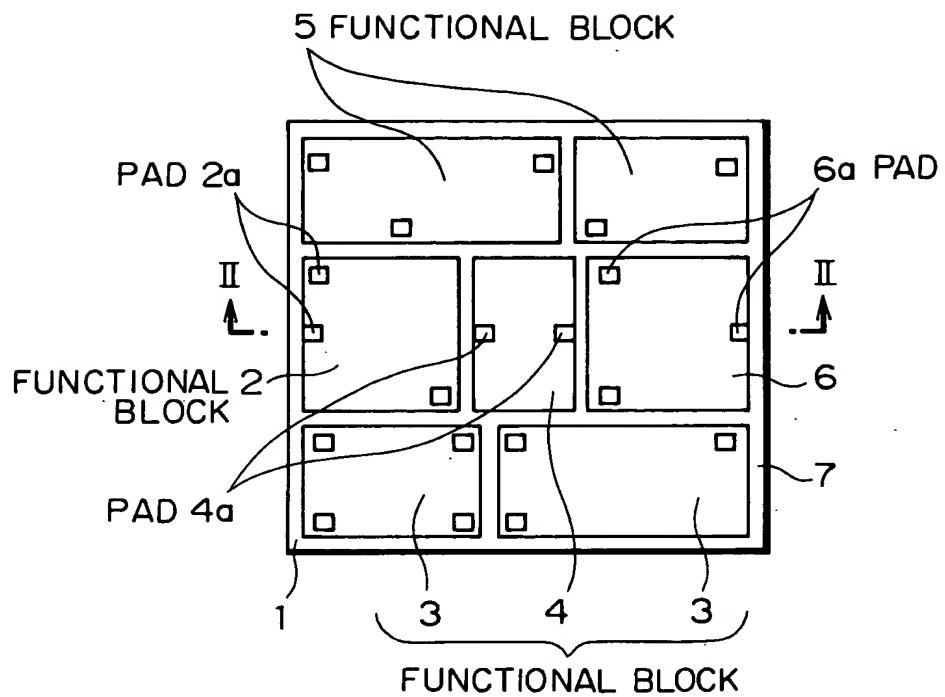


**FIG. IA**

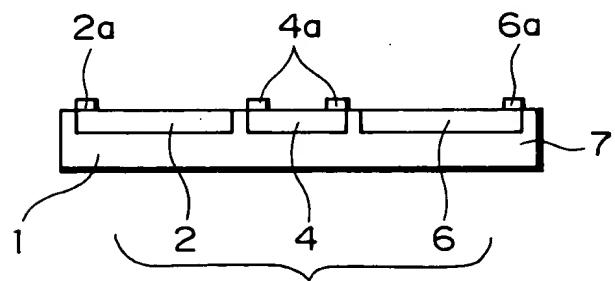


**FIG. IB**

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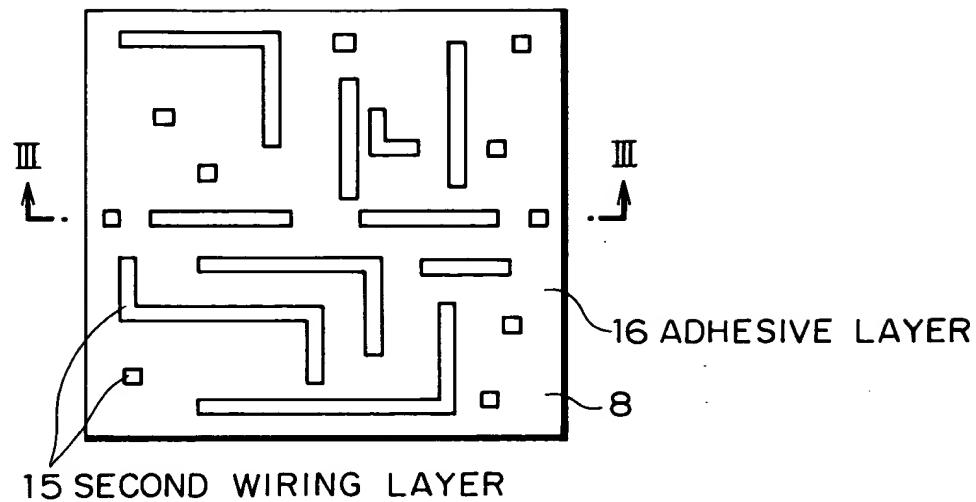


**FIG. 2A**

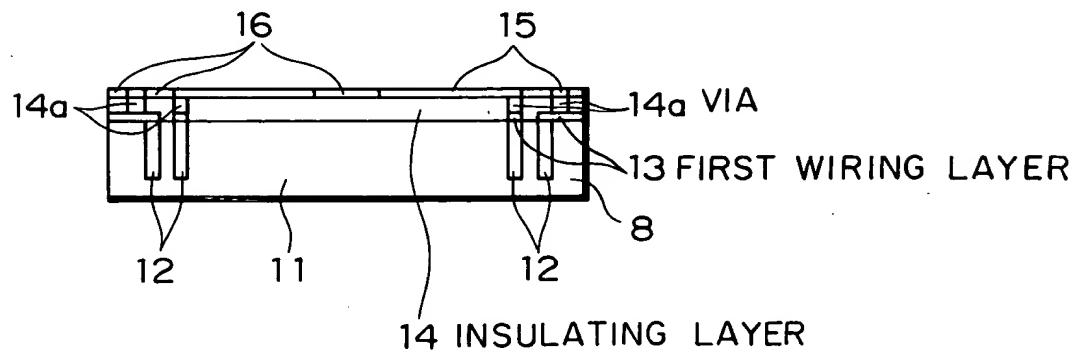


**FIG. 2B**

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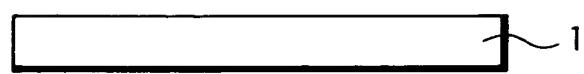


**FIG. 3A**

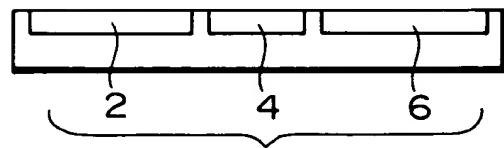


**FIG. 3B**

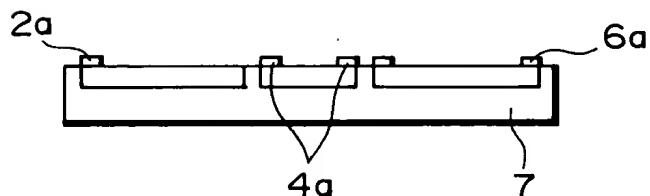
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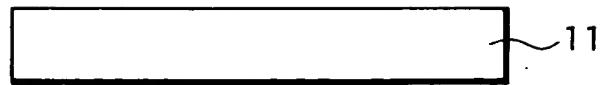
**FIG. 4A**



**FIG. 4B**



**FIG. 4C**



# FIG. 5A

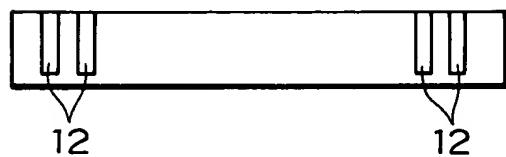


FIG. 5B

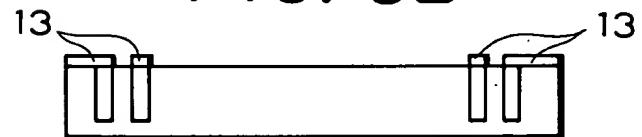
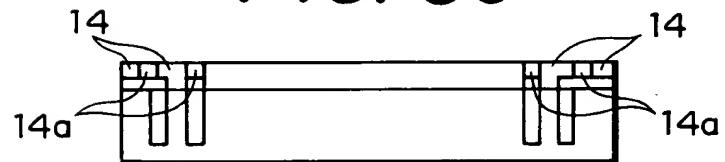
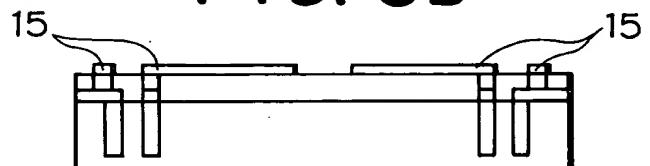


FIG. 5C



## FIG. 5D



**FIG. 5E**

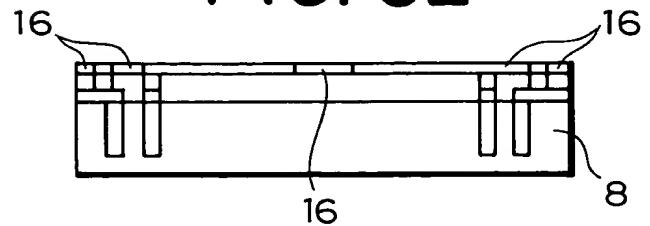
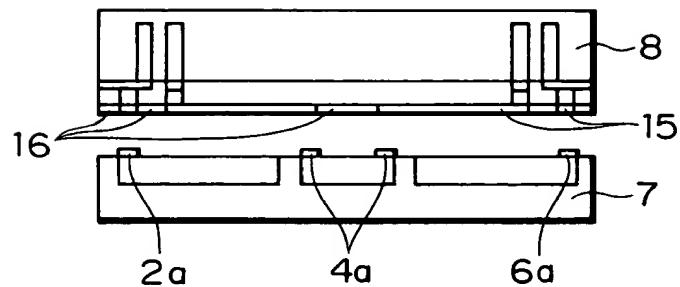
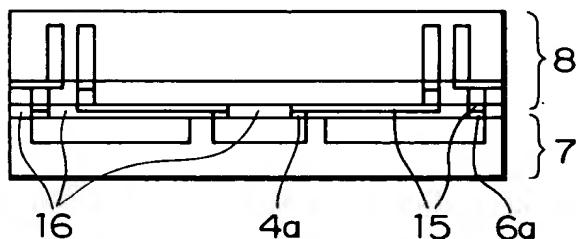


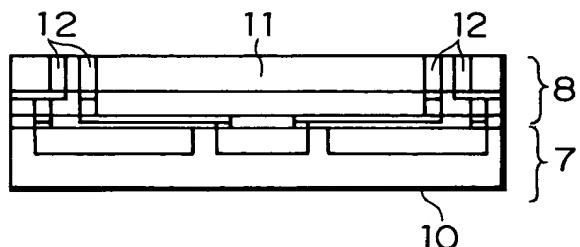
FIG. 5F



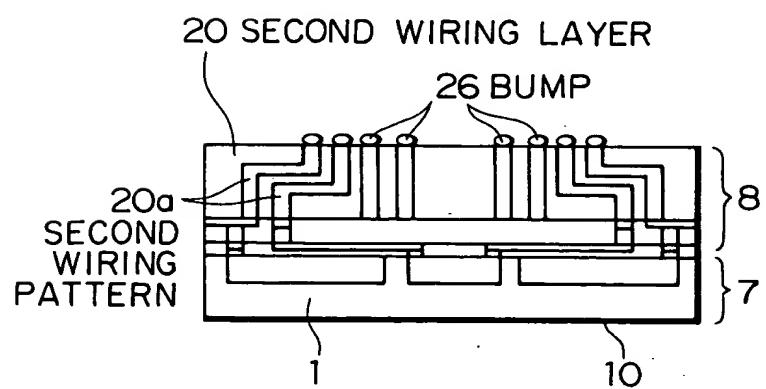
**FIG. 6A**



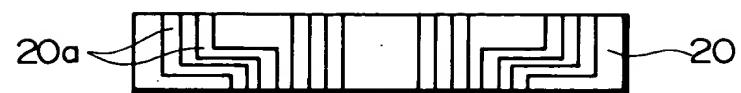
**FIG. 6B**



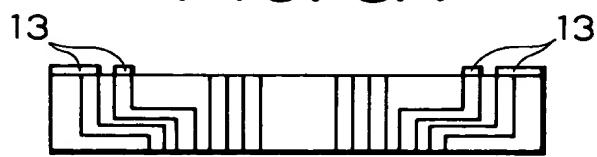
**FIG. 6C**



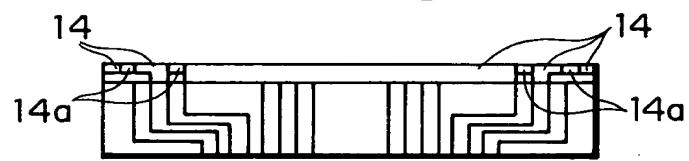
**FIG. 7**



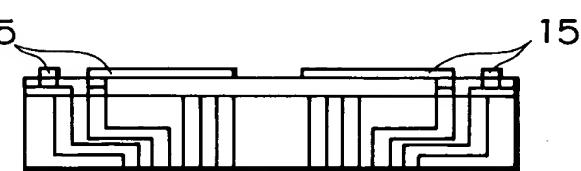
**FIG. 8A**



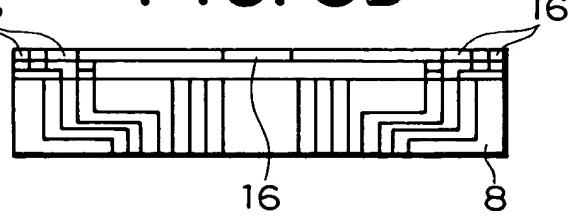
**FIG. 8B**



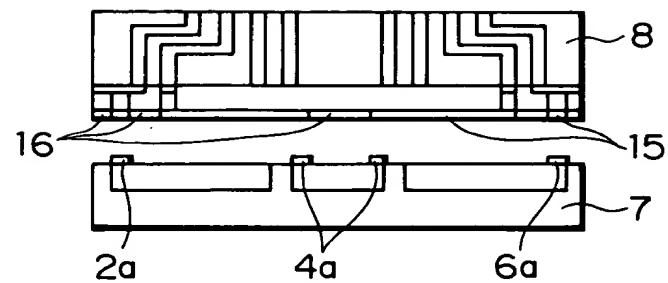
**FIG. 8C**



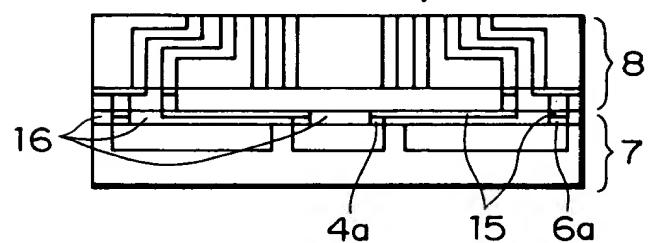
**FIG. 8D**



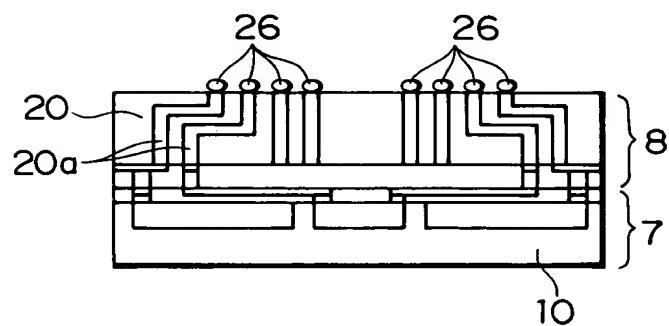
**FIG. 8E**



**FIG. 9A**



**FIG. 9B**



**FIG. 9C**

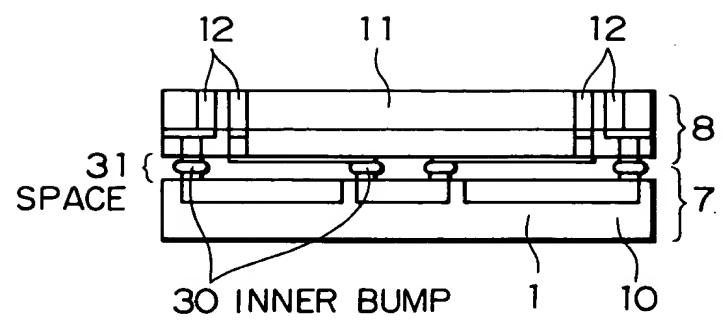
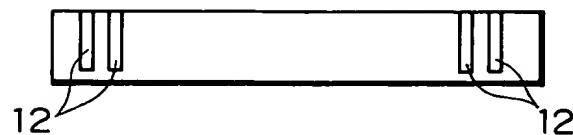


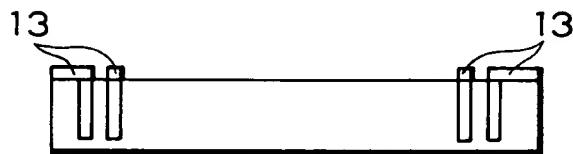
FIG. 10



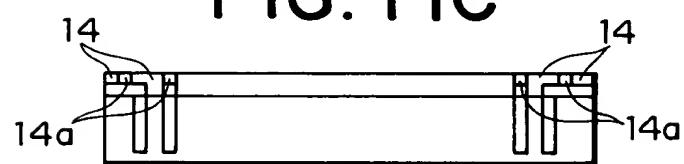
**FIG. I IA**



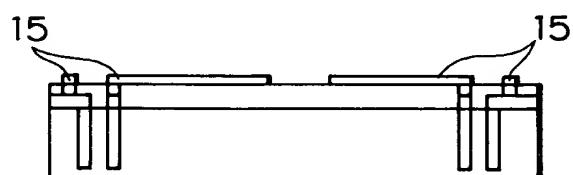
**FIG. I IB**



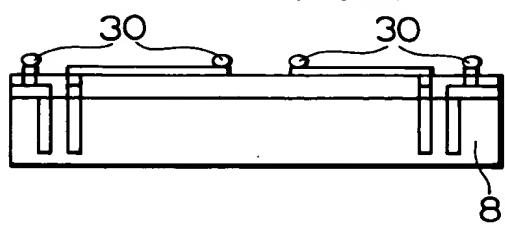
**FIG. I IC**



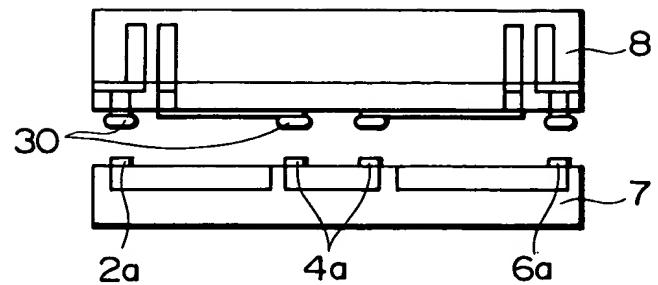
**FIG. I ID**



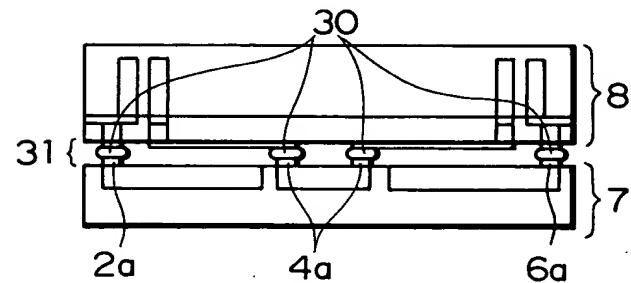
**FIG. I IE**



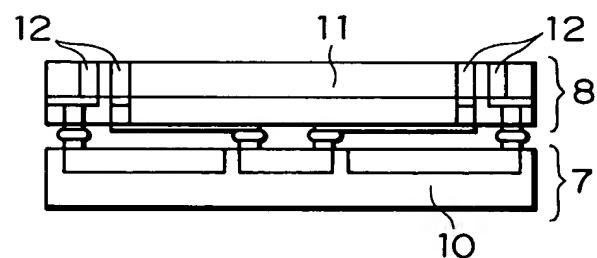
**FIG. I IF**



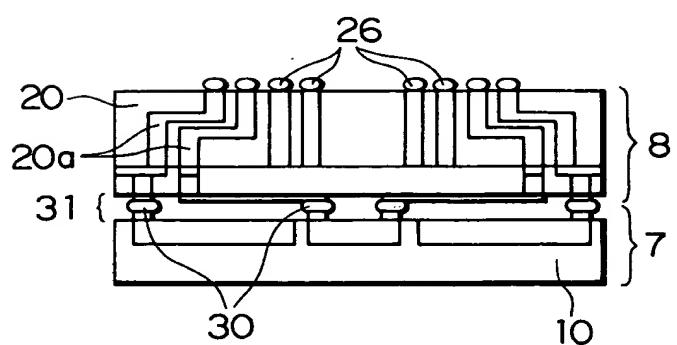
**FIG. 12A**



**FIG. 12B**



**FIG. 12C**



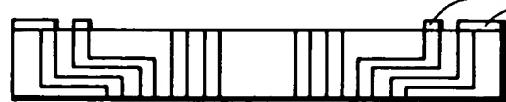
**FIG. 13**

wiring pattern

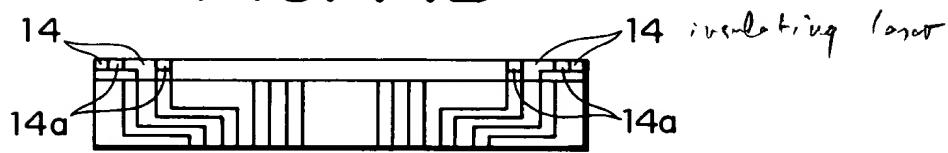


**FIG. 14A**

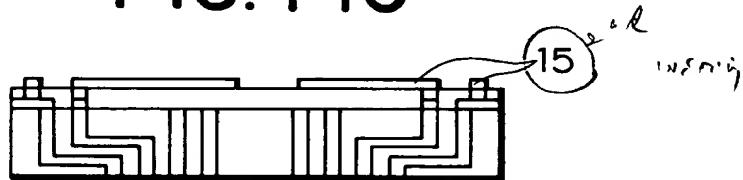
wiring layer



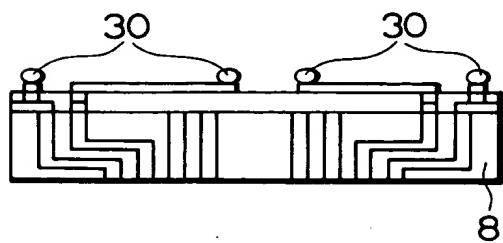
**FIG. 14B**



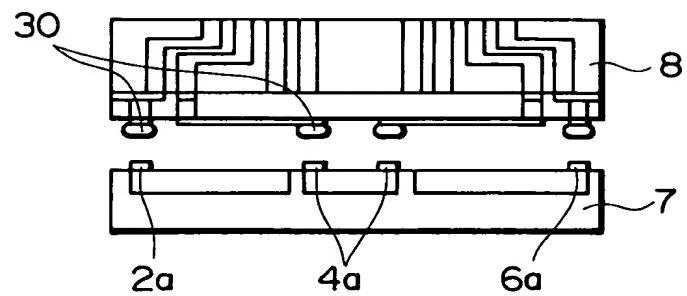
**FIG. 14C**



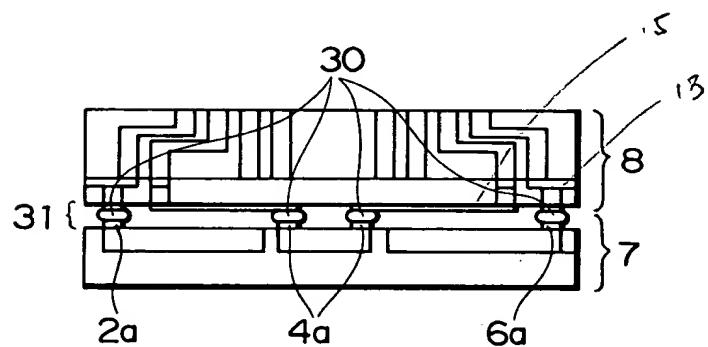
**FIG. 14D**



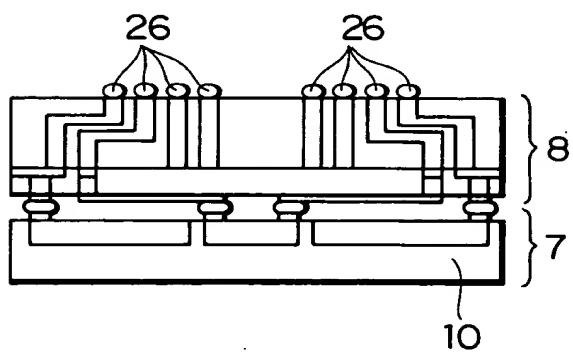
**FIG. 14E**



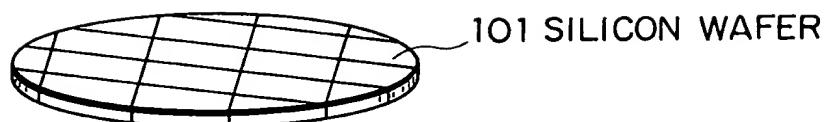
**FIG. 15A**



**FIG. 15B**



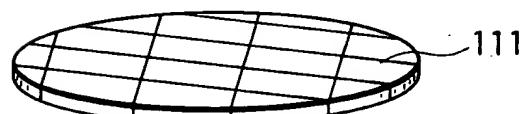
**FIG. 15C**



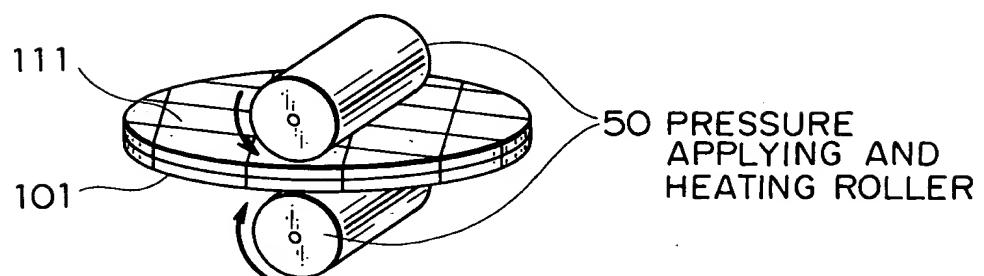
**FIG. 16A**



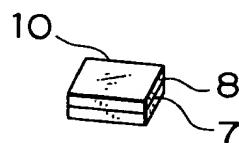
**FIG. 16B**



**FIG. 16C**



**FIG. 16D**



**FIG. 16E**